SPH01R9LM4H-1
MULTIMODE DIGITAL BOTTOM PORT SISONIC™ MICROPHONE

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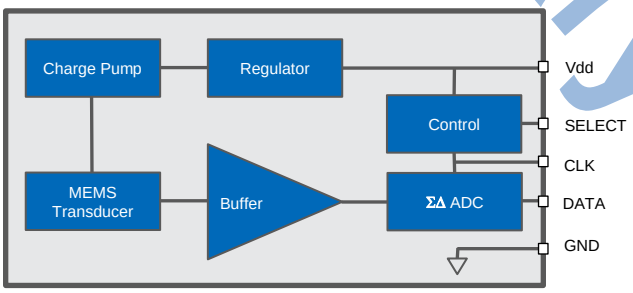
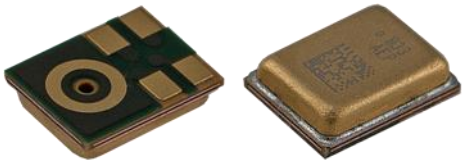
The SPH01R9LM4H-1 is a miniature, high-performance, low power, bottom port silicon digital microphone with a single bit PDM output. Using Syntiant's proven high performance SiSonic™ MEMS technology, the SPH01R9LM4H-1 consists of an acoustic sensor, a low noise input buffer, and a sigma-delta modulator. These devices are suitable for applications such as cellphones, smart phones, laptop computers, sensors, digital still cameras, portable music recorders, and other portable electronic devices where excellent wideband audio performance and RF immunity are required. In addition, the SPH01R9LM4H-1 offers multiple performance modes.





PRODUCT FEATURES

- Low Distortion /High AOP
- High SNR
- Low Current Consumption in Low-Power Mode
- Flat Frequency Response
- High Drive Capability
- RF Shielded
- Bottom Port
- Sensitivity Matching
- Supports Dual Multiplexed Channels
- Multiple Performance Modes (Sleep, Low-Power, Normal)
- Ultra-Stable Performance
- Omnidirectional
- Standard SMD Reflow
- LGA Package

TYPICAL APPLICATIONS

- Cellphones
- Headsets
- IOT devices
- Portable Electronics
- Laptop Computers
- Tablets

ABSOLUTE MAXIMUM RATINGS

Table 1: Absolute Maximum Ratings

Parameter	Absolute Maximum Rating	Units
Vdd to Ground	-0.5, +5.0	V
DATA, CLOCK, SELECT to Ground	-0.3, +5.0	V
Input Current	±5	mA
Short Circuit to/from DATA	Indefinite to Ground or Vdd	sec
Storage Temperature	-40 to +105	ºC
Operating Temperature	-40 to +105	ºC

Stresses exceeding these “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation at these or any other conditions beyond those indicated under “Acoustic & Electrical Specifications” is not implied. Exposure beyond those indicated under “Acoustic & Electrical Specifications” for extended periods may affect device reliability.

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ACOUSTIC & ELECTRICAL SPECIFICATIONS[1]

Table 2: General Microphone Specifications

Test Conditions: 25°C, 55±20% R.H., Vdd=1.8V, Vio=1.2V,Tedge ≤ 3ns, unless otherwise indicated

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	Vdd		1.62	1.8	1.98	V
Low Frequency Rolloff	LFRO	-3dB relative to 1 kHz	-	32	-	Hz
High Frequency Flatness		+3dB relative to 1 kHz	-	21	-	kHz
Resonant Frequency Peak	Fres	Free Field response	-	36	-	kHz
Latency			-		-	µs
DC Offset			-0.78	-	0.78	%
Directivity			Omnidirectional			
Polarity		Increasing sound pressure	Increasing density of 1's			
Data Format			½ Cycle PDM			
Sensitivity Drop		Vdd(min) ≤ Vdd ≤ Vdd(max)	-	-	TBD	dB
Clock Input Capacitance	Cin		-	TBD	-	pF
Data Output Capacitance	Cout		-	TBD	-	pF
Data Output Load	Cload		-	-	TBD	pF
SELECT (high)			0.7xVdd	-	Vdd+0.3	V
SELECT (low)			-0.3	-	0.3xVdd	V
Short Circuit Current	Isc	Grounded DATA pin	TBD	-	TBD	mA
Fall-asleep Time[3,4]		Fclock < 250kHz	-	-	10	ms
Wake-up Time[3,5]		Fclock ≥ 500kHz	-	-	35	ms
Startup Time[3]		Powered Down → Active, S within 1 dB of final value	-	-	35	ms
Time to First Data Bit[6]		Time from valid Vdd and CLK until the first logical bit is driven on the DATA line. The output is tristate until First Data Bit. Initial output bits represent muted audio. Audio data will follow Startup Time.	-	4	-	ms
Mode-Change Time[3, 6]		Low Power Mode ⇔ Normal Mode	-	-	20	ms

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Table 3: Normal Mode

Test Conditions: 25°C, 55±20% R.H., Vdd=1.8V, Vio=1.2V, Fclock = 2.4 MHz (D.C. = 50%), Tedge ≤ 3ns, SELECT grounded, no load, unless otherwise indicated

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Current[2]	Idd	Fclock = 2.4 MHz	-	650	-	µA
Sensitivity	S	94 dB SPL @ 1 kHz	-38	-37	-36	dBFS
Signal to Noise Ratio	SNR	Fclock = 2.4MHz, 94 dBSPL @ 1 kHz, A-weighted	-	65.7	-	dB(A)
Near-Ultrasonic SNR		94 dB SPL, @ 19 kHz , BW = 18.5 - 20.0 kHz	-	77.5	-	dB
Total Harmonic Distortion	THD	94 dB SPL @ 1 kHz	-	0.05	-	%
		1% THD @ 1 kHz, S = typ	-	130	-	dB SPL
Acoustic Overload Point	AOP	10% THD @ 1 kHz, S = typ	-	132	-	dB SPL
Power Supply Rejection Ratio	PSRR	200 mVpp sinewave @ 1 kHz	-	97	-	dB V/FS

Table 4: Low-Power Mode

Test Conditions: 25°C, 55±20% R.H., Vdd=1.8V, Vio=1.2V, Fclock = 768 kHz (D.C. = 50%), Tedge ≤ 3ns, SELECT grounded, no load, unless otherwise indicated

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Current[2]	Idd		-	240	-	µA
Sensitivity	S	94 dB SPL @ 1 kHz	-28	-27	-26	dBFS
Signal to Noise Ratio	SNR	94 dB SPL @ 1 kHz, A-weighted (BW = 8 kHz)	-	63	-	dB(A)
Total Harmonic Distortion	THD	94 dB SPL @ 1 kHz	-	0.05	-	%
		1% THD @ 1 kHz, S = typ	-	120	-	dB SPL
Acoustic Overload Point	AOP	10% THD @ 1 kHz, S = typ	-	122	-	dB SPL
Power Supply Rejection Ratio	PSRR	200 mVpp sinewave @ 1 kHz	-	90	-	dBV/FS

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Table 5: Sleep Mode

Test Conditions: 25°C, 55±20% R.H., Vdd=1.8V, Vio=1.2V, Fclock=0Hz, SELECT grounded, no load, unless otherwise indicated

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Sleep Current	Isleep		-	-	TBD	µA

[1] Sensitivity and Supply Current are 100% tested.
[2] Power consumption varies with Cload according to: ΔP = 1/3*Vio*Vio*ΔCload*Fclock.
[3] Valid microphones states are: Powered Down Mode (mic off), Sleep Mode (low current, DATA = high-Z, fast startup), Low-Power Mode (low clock speed) and Normal Mode.
[4] Time from Fclock < 5 kHz to Isleep specification is met when transitioning from Active Mode to Sleep Mode.
[5] Time from Fclock ≥ 320 kHz to all applicable specifications are met when transitioning from Sleep Mode to Active Mode.
[6] Audio is temporarily muted during the transition between any microphone state.

Table 6: Digital Interface

Test Conditions: 25°C, 55±20% R.H., Vdd=1.8V, Vio=1.2V, Tedge ≤ 3ns, unless otherwise indicated

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Clock stable high voltage[9]	Vstable-H	1.2Vio operation 1.8Vio operation	1.08 1.62	1.2 1.8	1.32 -	V
Clock stable low voltage[9]	Vstable-L	1.2Vio operation 1.8Vio operation	- -	0 0	0.12 0.18	V
Logic Input High[7, 8]	Vih	1.2Vio operation 1.8Vio operation	- -	- -	0.84 0.7xVDD	V
Logic Input Low[7, 8]	Vil	1.2Vio operation 1.8Vio operation	0.36 0.3xVDD	- -	- -	V
Logic Output High[7, 8]	Voh	I_{OUT} = 2 mA, 1.2Vio configuration I_{OUT} = 2 mA, 1.8Vio configuration	0.9 0.75xVDD	- -	- -	V
Logic Output Low[7, 8]	Vol	I_{OUT} = 2 mA, 1.2Vio configuration I_{OUT} = 2 mA, 1.8Vio configuration	- -	- -	0.3 0.25xVDD	V
Hysteresis Width[8]	Vhyst	1.2Vio operation 1.8Vio operation	0.12 0.1xVDD	- -	0.6 0.5xVDD	V
Clock Frequency[7]	Fclock	Sleep Mode	0	-	5	kHz
		Low-Power Mode	320	-	825	kHz
		Normal Mode	0.97	-	3.3	MHz
Clock Duty Cycle	D.C.		40	50	60	%
Delay Time to Data Line Driven[7]	Tdd		18	-	35	ns
Delay Time to Valid Data[7]	Tdv	Max Cload	-	-	123	ns
Delay Time to High Z[7]	Tdz		5	-	16	ns
Hold Time[7]	Thold	dependent on Cload as observed by the input device	5	-	-	ns

[7] See Figure 1: Timing Diagram.
[8] See Figure 2: Hysteresis Diagram.
[9] See Figure 6: CLOCK Domain Auto Detection Requirements.

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Figure 1: Timing Diagram

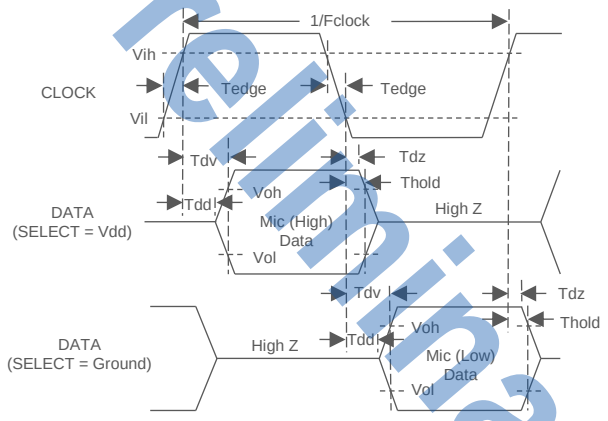


Figure 2: Hysteresis Diagram

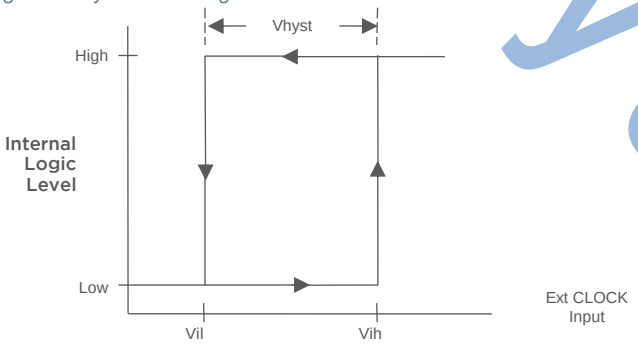


Figure 3: State Diagram

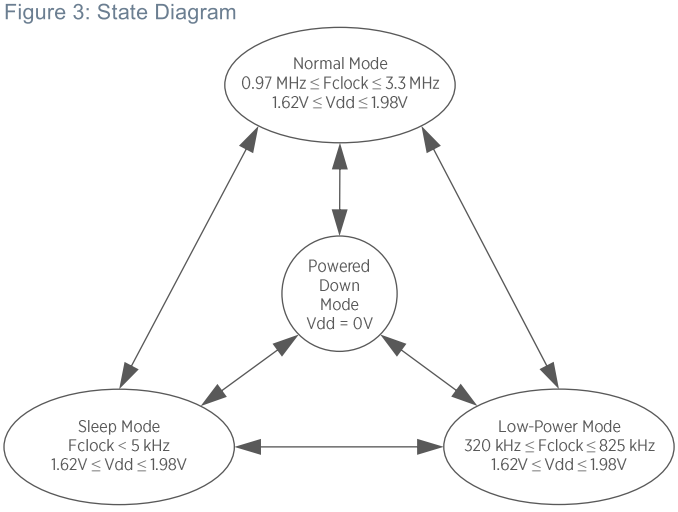


Figure 4: Typical Stereo Application Circuit

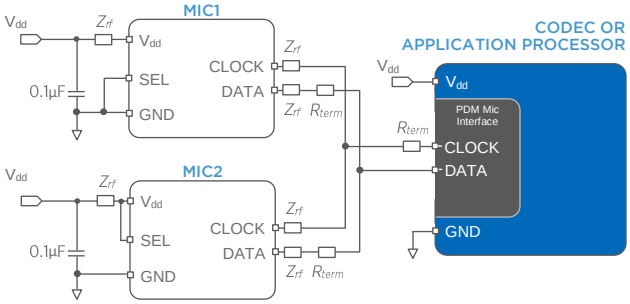
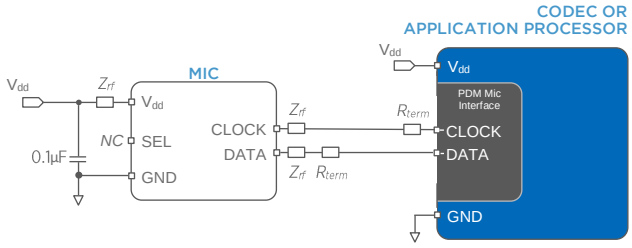


Figure 5: Typical Single-Microphone Application Circuit



NOTES:

All Ground pins must be connected to ground.
If necessary to improve RF performance, optional series components (resistors, ferrites, etc.) should be placed closest to the microphone pads.
Bypass capacitors should be placed near each Vdd pin for best performance.
Capacitors near the microphone should not contain Class 2 dielectrics due to their piezoelectric effect.

Figure 6: CLOCK Domain Auto Detection Requirements

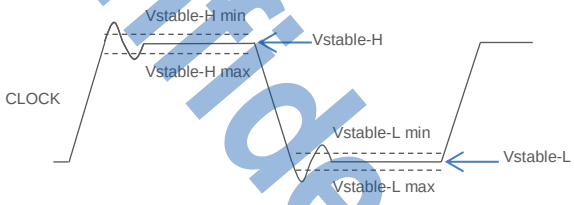


Table 7: SELECT Functionality

Microphone	SELECT	Asserts DATA on	Latch DATA on
Mic (High)	Vdd	CLK rising edge	CLK falling edge
Mic (Low)	Ground	CLK falling edge	CLK rising edge

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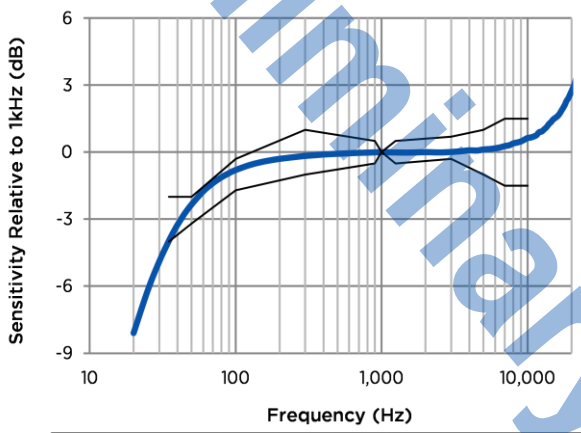
PERFORMANCE CURVES

Test Conditions: 23 ±2°C, 55±20% R.H., Vdd=1.8 V, Fclock = 2.4 MHz, SELECT grounded, no load, unless otherwise indicated

Figure 6: Typical Free Field Magnitude and Masks



	35	50	100	300	900	1000	1250	3000	5000	7000	10000
USL	-2	-2	-0.3	1	0.5	0	0.5	0.7	1	1.5	1.5
LSL	-4	-3.2	-1.7	-1	-0.5	0	-0.5	-0.3	-1	-1.5	-1.5

Figure 7: Typical THD vs SPL

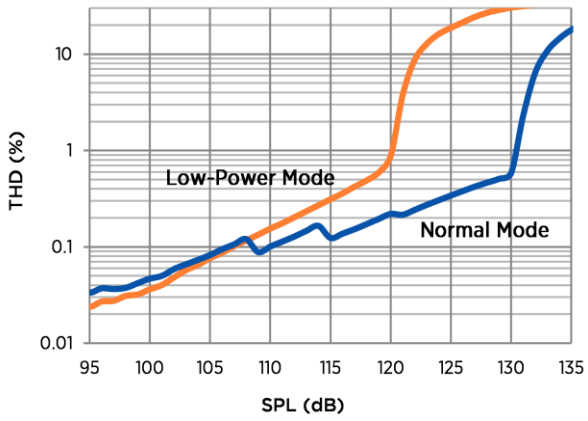
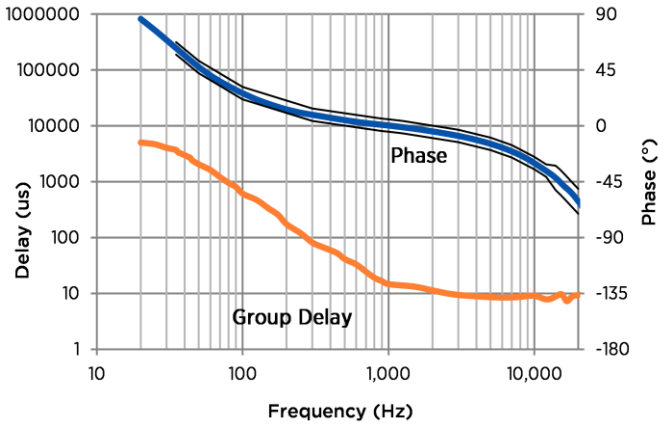


Figure 8: Typical Phase and Group Delay



Tolerance	35	50	100	300	900	1000	1250	3000	5000	7000	10000	12000	14000	15000	16000	20000
USL	5	5	5	5	5	5	5	5	5	5	5	5	10	10	10	10
LSL	-5	-5	-5	-5	-5	-5	-5	-5	-5	-5	-5	-5	-10	-10	-10	-10

Figure 9: Typical THD vs Frequency

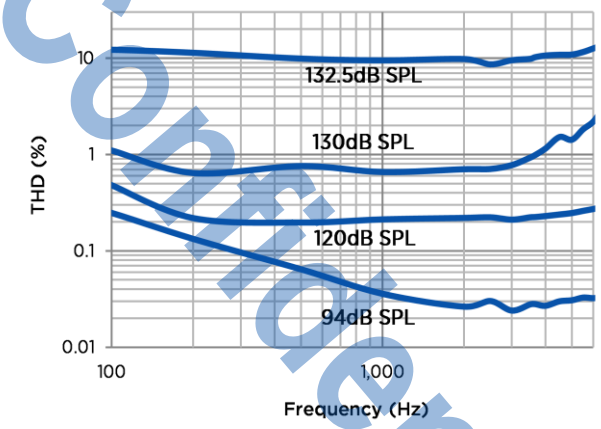


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Figure 10: Typical Free Field Ultrasonic Response

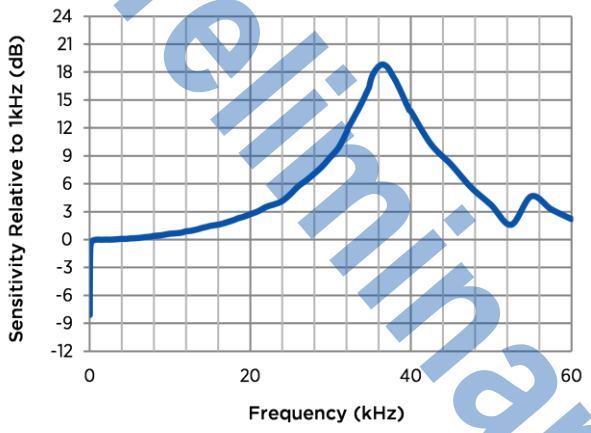


Figure 11: Typical Idd vs Vdd

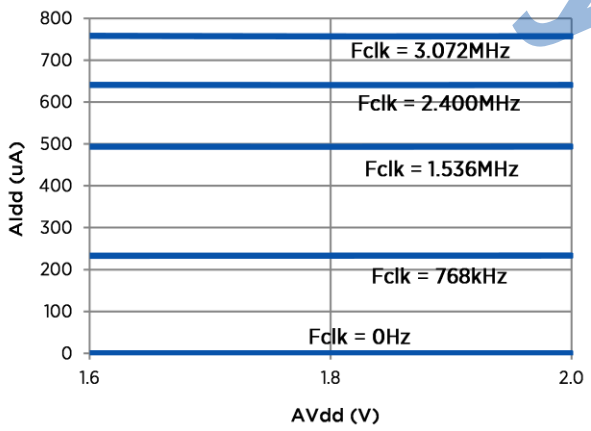


Figure 12: Noise Floor Power Spectral Density

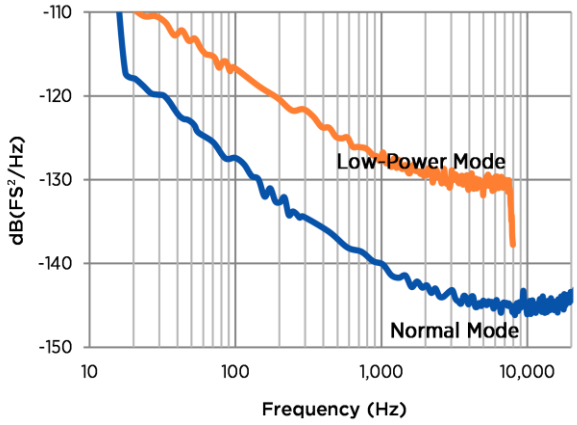
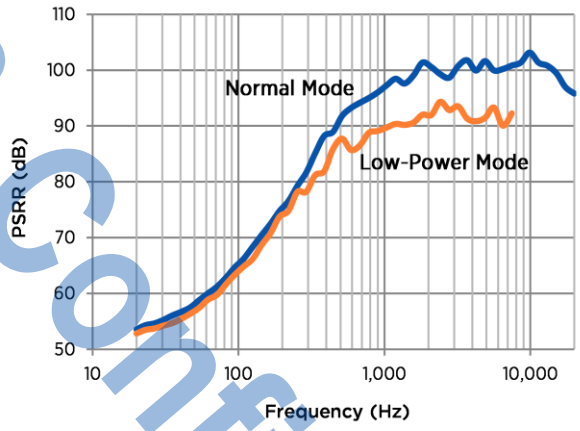


Figure 13: Typical PSRR



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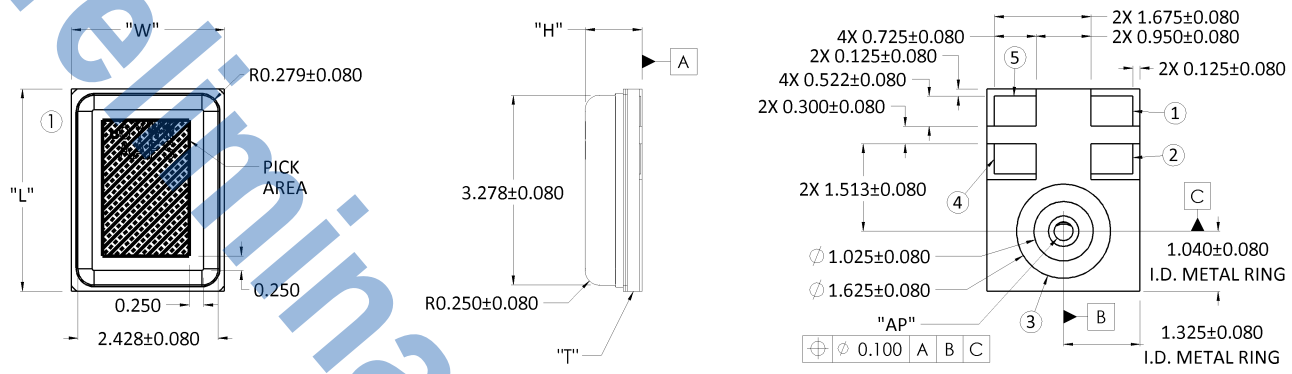
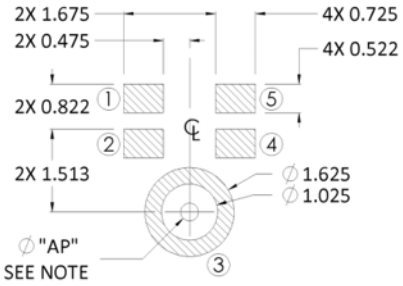
MECHANICAL SPECIFICATIONS



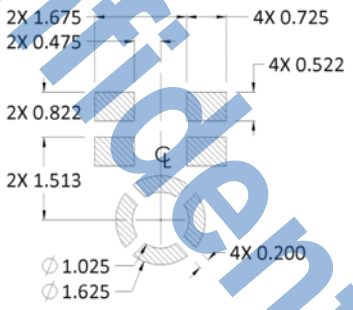
Item	Dimension	Tolerance
Length (L)	3.5	±0.10
Width (W)	2.65	±0.10
Height (H)	0.8	±0.10
Acoustic Port (AP)	Ø0.325	±0.05
PCB Thickness (T)	0.3	±0.05

Pin #	Pin Name	Type	Description
1	DATA	Digital O	PDM Output
2	SELECT	Digital I	Lo/Hi (L/R) Select Connect to Vdd or GND
3	GROUND	Power	Ground
4	CLOCK	Digital I	Clock Input
5	Vdd	Power	Power Supply: Do not connect to GND while CLOCK is applied.

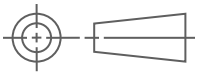
Example Land Pattern



Example Solder Stencil Pattern



NOTES:



Pick Area only extends to 0.25 mm of any edge or hole unless otherwise specified.
Dimensions are in millimeters unless otherwise specified.
Tolerance is ±0.15mm unless otherwise specified
Maximum force applied to microphone package:

- Transient 50N max applied to entire metal can top area. 10N max point force (spherical push pin 1mm radius)
- Static 10N max on entire can top area.

In the acoustic path, the recommended PCB Hole Diameter is 0.475 ≤ D ≤ 0.625mm, the recommended Gasket Cavity Diameter is D ≥ 1.0mm and the recommended Case Hole Diameter is 1.0 ≤ D ≤ 1.5mm. Further optimizations based on application should be performed.

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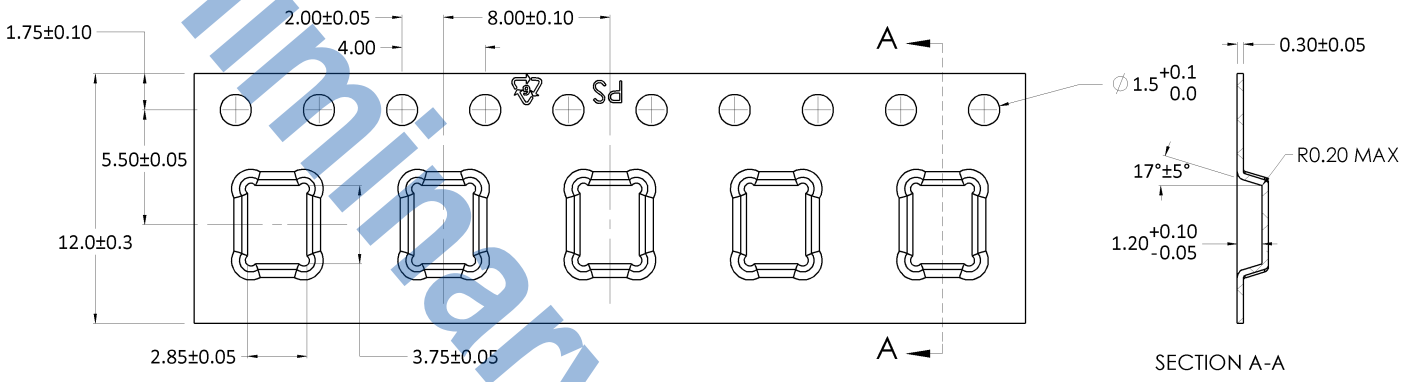
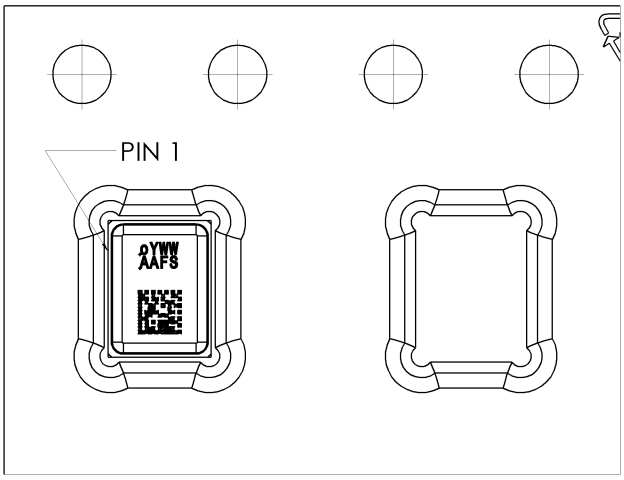
PACKAGING & MARKING DETAIL



Model Number	Suffix	Reel Diameter	Quantity Per Reel
SPH01R9LM4H-1	-8	13”	5900

Component	Surface Resistance (ohms)
Reel	10^5 - 10^9
Carrier Tape	10^5 - 10^9
Cover Tape	10^4 - 10^{10}



Letter: “o”, orientation mark (pin 1)
YWWAAF = Internal Code
2D barcode "ABCDEFGHJKLMNPQRSTUVWXYZ0123456789":
Unique Job Identification Number for product traceability

NOTES:

Dimensions are in millimeters unless otherwise specified.
Vacuum pickup only in the pick area indicated in Mechanical Specifications.
Tape & reel per EIA-481.
Labels applied directly to reel and external package.
Shelf life: Twelve (12) months when devices are stored in the factory-supplied, unopened ESD moisture sensitive bag under the maximum environmental conditions of 30°C, 70% R.H.

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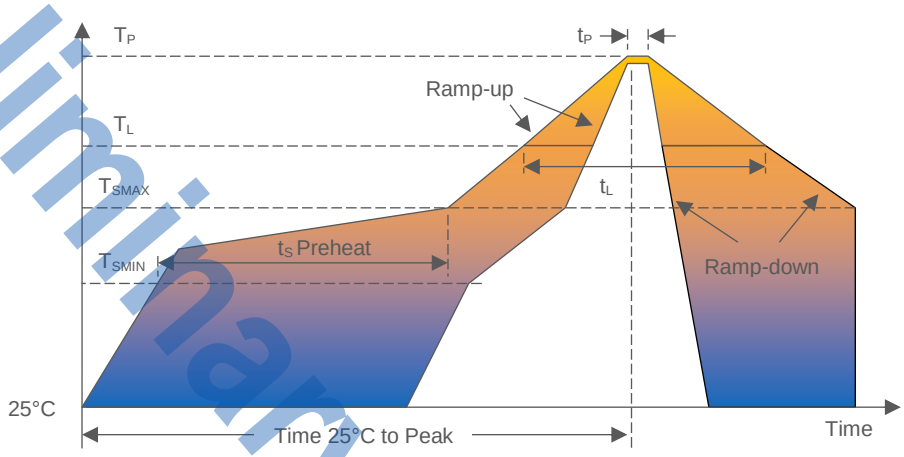
RECOMMENDED REFLOW PROFILE



Profile Feature	Pb-Free
Average Ramp-up rate (T_{SMAX} to T_P)	3°C/second max.
Preheat • Temperature Min (T_{SMIN}) • Temperature Max (T_{SMAX}) • Time (T_{SMIN} to T_{SMAX}) (t_S)	 150°C 200°C 60-180 seconds
Time maintained above: • Temperature (T_L) • Time (t_L)	 217°C 60-150 seconds
Peak Temperature (T_P)	260°C
Time within 5°C of actual Peak Temperature (t_P)	20-40 seconds
Ramp-down rate (T_P to T_{SMAX})	6°C/second max
Time 25°C to Peak Temperature	8 minutes max

NOTES:

Based on IPC/JDEC J-STD-020 Revision C.

All temperatures refer to topside of the package, measured on the package body surface.

The actual reflow profile used should be optimized based on the reflow requirements of all components, board design, solder paste formulation and reflow equipment used. Details of recommended handling and manufacturing processes can be found in AN25 SMT Manufacturing Guidelines for SiSonic™ Microphones.

ADDITIONAL NOTES

(A) MSL (moisture sensitivity level) Class 1.
(B) Maximum of 3 reflow cycles is recommended.
(C) In order to minimize device damage:
- Do not board wash or clean after the reflow process.
- Do not brush board with or without solvents after the reflow process.
- Do not directly expose to ultrasonic processing, welding, or cleaning.
- Do not insert any object in port hole of device at any time.
- Do not apply over 30 psi of air pressure into the port hole.
- Do not pull a vacuum over port hole of the microphone.
- Do not apply a vacuum when repacking into sealed bags at a rate faster than 0.5 atm/sec.
- Do not directly expose to vapor phase soldering.

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MATERIALS STATEMENT

Meets the requirements of the European RoHS directive 2011/65/EC as amended.

Meets the requirements of the industry standard IEC 61249-2-21:2003 for halogenated substances and Syntiant Green Materials Standards Policy section on Halogen-Free.

Product is Beryllium Free according to limits specified on the Syntiant Hazardous Material List (HSL for Products).

Ozone depleting substances are not used in the product or the processes used to make the product, including compounds listed in Annex A, B, and C of the “Montreal Protocol on Substances That Deplete the Ozone Layer.

RELIABILITY SPECIFICATIONS

Test	Description
Thermal Shock	100 cycles of air-air thermal shock from -40°C to +125°C with 15 minute soaks (IEC 68-2-14)
High Temperature Storage	+105°C environment for 1,000 hours (IEC 68-2-2 Test Ba)
Low Temperature Storage	-40°C environment for 1,000 hours (IEC 68-2-1 Test Aa)
High Temperature Bias	+105°C environment while under bias for 1,000 hours (IEC 68-2-2 Test Ba)
Low Temperature Bias	-40°C environment while under bias for 1,000 hours (IEC 68-2-1 Test Aa)
Temperature/Humidity Bias	+85°C/85% R.H. environment while under bias for 1,000 hours (JESD22-A101A-B)
Vibration	12 minutes in each X, Y, Z axis from 20 to 2,000 Hz with peak acceleration of 20g (MIL STD-883e, Method 2007.2, Condition A)
ESD-HBM	3 discharges at ±2kV direct contact to I/O pins (ESD STM5.2)
ESD-LID/GND	3 discharges at ±8kV direct contact to lid when unit is grounded (IEC 61000-4-2)
Reflow	5 reflow cycles with peak temperature of +260°C (JEDEC 22-A113F)
Mechanical Shock	3 pulses of 10,000g in each of the X, Y, and Z directions (IEC 68-2-27 Test Ea)

NOTES:

Microphones meet all acoustic and electrical specifications before and after reliability testing, except sensitivity which can deviate up to 3dB.

After 3 reflow cycles, the sensitivity of the microphones shall not deviate more than 1 dB from its initial value.

Temperature Storage testing is covered by Temperature Bias testing as Ta = Tj for Syntiant Microphones.

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SPECIFICATION REVISIONS

Revision	Specification Changes	Date
1	Initial draft	5/13/2024
2	Updated some images and max Vih	7/12/2024
3	Updated digital interface specs	8/7/2024
4	Added diagram showing clock domain auto detection requirements	8/22/2024
5	Updated can height	9/25/2024
6	Syntiant document format update	11/22/2024
7	Updated SNR, AOP and LFRO	1/13/2025
8	Updated LFRO	1/16/2025

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